CIS 429/529

The IBM Legacy

Prof. Michel A. Kinsky
The IBM 650 (1953-4)

Magnetic Drum (1,000 or 2,000 10-digit decimal words)

Active instruction (including next program counter)

20-digit accumulator

Digit-serial ALU

[From 650 Manual, © IBM]
IBM 650: A drum machine with 44 instructions

- Instruction: \[60 \ 1234 \ 1009\]
  - “Load the contents of location 1234 into the distribution; put it also into the upper accumulator; set lower accumulator to zero; and then go to location 1009 for the next instruction.”

- Programmer’s view of the machine was inseparable from the actual hardware implementation

- Good programmers optimized the placement of instructions on the drum to reduce latency!
Compatibility Problem at IBM

• By early 60’s, IBM had 4 incompatible lines of computers!
  ▶ 701 → 7094
  ▶ 650 → 7074
  ▶ 702 → 7080
  ▶ 1401 → 7010

• Each system had its own
  ▶ Instruction set
  ▶ I/O system and Secondary Storage:
Compatibility Problem at IBM

- By early 60’s, IBM had 4 incompatible lines of computers!

- Each system had its own
  - Instruction set
  - I/O system and Secondary Storage:
    - magnetic tapes, drums and disks
  - Assemblers, compilers, libraries,…
  - Market niche
    - business, scientific, real time, …
IBM 360: Design Premises

• Amdahl, Blaauw and Brooks, 1964

  ▶ The design must lend itself to growth and successor machines
  ▶ General method for connecting I/O devices
  ▶ Total performance - answers per month rather than bits per microsecond → programming aids
  ▶ Machine must be capable of supervising itself without manual intervention
IBM 360: Design Premises

- Amdahl, Blaauw and Brooks, 1964
  - Built-in hardware fault checking and locating aids to reduce down time
  - Simple to assemble systems with redundant I/O devices, memories etc. for fault tolerance
  - Some problems required floating point words larger than 36 bits
IBM 360: A GPR Machine

- A General-Purpose Register (GPR) Machine: Processor State
  - 16 General-Purpose 32-bit Registers
    - may be used as index and base register
    - Register 0 has some special properties
  - 4 Floating Point 64-bit Registers
  - A Program Status Word (PSW)
    - PC, Condition codes, Control flags
IBM 360: A GPR Machine

• A General-Purpose Register (GPR) Machine: Processor State
  ‣ A 32-bit machine with 24-bit addresses
    • No instruction contains a 24-bit address!
  ‣ Data Formats
    • 8-bit bytes, 16-bit half-words, 32-bit words, 64-bit double-words
IBM 360: Addressing Modes

- **RR**
  
  \[
  R1 \leftarrow (R1) \text{ op } (R2)
  \]

- **RD**
  
  \[
  R \leftarrow (R) \text{ op } M[(X) + (B) + D]
  \]
  
  A 24-bit address is formed by adding the 12-bit displacement (D) to a base register (B) and an index register (X), if desired.

- The most common formats for arithmetic & logic instructions, as well as Load and Store instructions.
IBM 360: String Operations

- SS format: store to store instructions
  - \[ M[(B1) + D1] \leftarrow M[(B1) + D1] \text{ op } M[(B2) + D2] \]
    iterate “length” times

<table>
<thead>
<tr>
<th>Opcode</th>
<th>length</th>
<th>B1</th>
<th>D1</th>
<th>B2</th>
<th>D2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>8</td>
<td>4</td>
<td>12</td>
<td>4</td>
<td>12</td>
</tr>
</tbody>
</table>

- Most operations on decimal and character strings use this format
  - MVC move characters
  - MP multiply two packed decimal strings
  - CLC compare two character strings
IBM 360: Control Flow

- Arithmetic and logic instructions set condition codes
  - equal to zero
  - greater than zero
  - overflow
  - carry…

- I/O instructions also set condition codes
  - channel busy
IBM 360: Control Flow

- Conditional branch instructions are based on testing condition code registers (CC’s)
  - RX and RR formats
    - BC_ branch conditionally
    - BAL_ branch and link, i.e., $R15 \leftarrow (PC)+1$
      for subroutine calls
    - CC’s must be part of the PSW
IBM 360: Precise Interrupts

- IBM 360 ISA (Instruction Set Architecture) preserves sequential execution model

- Programmers view of machine was that each instruction either completed or signaled a fault before next instruction began execution

- Exception/interrupt behavior constant across family of implementations
### IBM 360: 1964 Implementations

<table>
<thead>
<tr>
<th></th>
<th>Model 30</th>
<th>...</th>
<th>Model 70</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Capacity</td>
<td>8K - 64 KB</td>
<td>...</td>
<td>256K - 512 KB</td>
</tr>
<tr>
<td>Memory Cycle</td>
<td>2.0μs</td>
<td>...</td>
<td>1.0μs</td>
</tr>
<tr>
<td>Datapath</td>
<td>8-bit</td>
<td>...</td>
<td>64-bit</td>
</tr>
<tr>
<td>Circuit Delay</td>
<td>30 nsec/level</td>
<td></td>
<td>5 nsec/level</td>
</tr>
<tr>
<td>Registers in</td>
<td>Main Store</td>
<td></td>
<td>in Transistor</td>
</tr>
<tr>
<td>Control Store</td>
<td>Read only 1μsec</td>
<td></td>
<td>Dedicated circuits</td>
</tr>
</tbody>
</table>

- Six implementations (Models, 30, 40, 50, 60, 62, 70)
- 50X performance difference cross models
- ISA completely hid the underlying technological differences between various models
  - With minor modifications, IBM 360 ISA is still in use
IBM 360: Forty years later...

- The zSeries z990 Microprocessor
  - 64-bit virtual addressing
    - original 360 was 24-bit; 370 was a 31-bit extension
  - Dual core design
  - Dual-issue in-order superscalar
  - 10-stage CISC pipeline
  - Out-of-order memory accesses
  - Redundant datapaths
    - every instruction performed in two parallel datapaths and results compared

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IBM 360: Forty years later…

• The zSeries z990 Microprocessor
  ‣ 256KB L1 I-cache, 256KB L1 D-cache on-chip
  ‣ 32MB shared L2 unified cache, off-chip
  ‣ 512-entry L1 TLB + 4K-entry L2 TLB
    • very large TLB, to support multiple virtual machines
  ‣ 8K-entry Branch Target Buffer
    • Very large buffer to support commercial workloads
  ‣ Up to 64 processors (48 visible to customer) in one machine
  ‣ 1.2 GHz in IBM 130nm SOI CMOS technology, 55W for both cores