CIS 314

RISC vs. CISC ISAs

Prof. Michel A. Kinsky
Complex Instruction Set Computer

- Large number of instructions (~200-300 instructions)
  - Small code sizes
- Specialized complex instructions
  - Multi-clock instructions
- Many different addressing modes
  - Including specialized modes for indexing through arrays
Complex Instruction Set Computer

- Large number of instructions (~200-300 instructions)
- Specialized complex instructions
- Many different addressing modes
  - Including specialized modes for indexing through arrays
  - 12 addressing modes available in x86
    - Immediate, Register operand, Displacement, Base, Base with displacement, Scaled index with displacement, Base with index and displacement, Base scaled index with displacement and Relative
Complex Instruction Set Computer

- Large number of instructions (~200-300 instructions)
- Specialized complex instructions
- Many different addressing modes
- Variable length instruction format

<table>
<thead>
<tr>
<th>Instruction Prefixes</th>
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<th>Instruction Prefixes</th>
<th>Instruction Prefixes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 or 1</td>
<td>0 or 1</td>
<td>0 or 1</td>
<td>0 or 1</td>
<td>Bytes</td>
</tr>
<tr>
<td>Segment Override</td>
<td>Operand size Override</td>
<td>Address size Override</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0, 1, 2, 3, or 4 bytes</td>
<td>1 or 2</td>
<td>0 or 1</td>
<td>0 or 1</td>
<td></td>
</tr>
<tr>
<td>Opcode</td>
<td>ModR/M</td>
<td>SIB</td>
<td>Displacement</td>
<td>Immediate</td>
</tr>
<tr>
<td>Mod</td>
<td>Reg/Opcode</td>
<td>R/M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 6 5 4 3 2 1 0</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
Complex Instruction Set Computer

- Large number of instructions (~200-300 instructions)
- Specialized complex instructions
- Many different addressing modes
- Variable length instruction format
- Examples: 68000, 80x86, VAX, PDP-11
Complex Instruction Set Computer

- Large number of instructions (~200-300 instructions)
- Specialized complex instructions
- Many different addressing modes
- Variable length instruction format
- General advantages
  ‣ Each instruction is more capable
  ‣ Fewer instructions needed to implement a given task
  ‣ More efficient use of slow main memory
Complex Instruction Set Computer

- No extra load in accessing data in memory
- Easy encoding
- Operands being not equivalent
- Restricted number of registers due to encoding memory address
- Irregularity in CPI
Complex Instruction Set Computer

• Disadvantages
  ‣ Backward compatibility means with each new generation of computers instruction set and hardware become more and more complex
  ‣ Individual instructions could be of almost any length
    • Different instructions will take different amounts of clock time to execute
    • Slows down the overall performance of the machine
  ‣ Many specialized instructions are not used frequently enough to justify their existence
Disadvantages

- Many specialized instructions are not used frequently enough to justify their existence
  - Approximately 20% of the available instructions are used in a typical program
- CISC instructions typically set the condition codes as a side effect of the instruction
  - Setting the condition codes take time
  - Programmers must remember to examine the condition code bits before a subsequent instruction changes them
## 80x86 Instruction Frequency

<table>
<thead>
<tr>
<th>Rank</th>
<th>Instruction</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>load</td>
<td>22%</td>
</tr>
<tr>
<td>2</td>
<td>branch</td>
<td>20%</td>
</tr>
<tr>
<td>3</td>
<td>compare</td>
<td>16%</td>
</tr>
<tr>
<td>4</td>
<td>store</td>
<td>12%</td>
</tr>
<tr>
<td>5</td>
<td>add</td>
<td>8%</td>
</tr>
<tr>
<td>6</td>
<td>and</td>
<td>6%</td>
</tr>
<tr>
<td>7</td>
<td>sub</td>
<td>5%</td>
</tr>
<tr>
<td>8</td>
<td>register move</td>
<td>4%</td>
</tr>
<tr>
<td>9</td>
<td>call</td>
<td>1%</td>
</tr>
<tr>
<td>10</td>
<td>return</td>
<td>1%</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>96%</td>
</tr>
</tbody>
</table>
Reduced Instruction Set Computer

- Relatively few number of instructions (~50)
- Basic instructions
- Relatively few different addressing modes
- Fixed length instruction format
- Only load/store instructions can access memory
- Large number of registers
- Hardwired rather than micro-program control
Reduced Instruction Set Computer

- Simpler to design
- Higher Performance
  - Smaller die size
- Lower power consumption
- Easier to develop compilers to take advantage of all features
  - Simple code generation
  - Regularity in CPI
Reduced Instruction Set Computer

- RISC ISA is extensively used for desktop, server, and embedded: MIPS, PowerPC, UltraSPARC, ARM, MIPS16, Thumb
  - Apple iPods (custom ARM7TDMI SoC)
  - Apple iPhone (Samsung ARM1176JZF)
  - Palm and PocketPC PDAs and smartphones (Intel XScale family, Samsung SC32442 - ARM9)
  - Nintendo Game Boy Advance (ARM7)
  - Nintendo DS (ARM7, ARM9)
Reduced Instruction Set Computer

• Disadvantages
  ‣ Higher instruction counts
  ‣ Lower instruction density
  ‣ Put a greater burden on the software or system programmer
# CISC & RISC Summary

<table>
<thead>
<tr>
<th>Year</th>
<th>Instr.</th>
<th>Instr. Size</th>
<th>Addr Modes</th>
<th>Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM 370/168</td>
<td>1973</td>
<td>208</td>
<td>2 - 6</td>
<td>4</td>
</tr>
<tr>
<td>VAX 11/780</td>
<td>1978</td>
<td>303</td>
<td>2 - 57</td>
<td>22</td>
</tr>
<tr>
<td>I 80486</td>
<td>1989</td>
<td>235</td>
<td>1 - 11</td>
<td>11</td>
</tr>
<tr>
<td>M 88000</td>
<td>1988</td>
<td>51</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>MIPS R4000</td>
<td>1991</td>
<td>94</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>IBM 6000</td>
<td>1990</td>
<td>184</td>
<td>4</td>
<td>2</td>
</tr>
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</table>
Next Class

• MIPS & x86