Team names:

Overview
For this assignment, you will learn how to write RTL and become familiar with the design tools you will use throughout the term. You are encouraged to form teams of 3 and to discuss the design with other students in the class.

Project
Implement a GCD algorithm that is able to handle unsigned 8-bit numbers.

```java
//Euclidean algorithm
function gcd(a:int,b:int):int
{
    var tmp:int;
    //Swap the numbers so a >= b
    if(a < b)
    {
        tmp = a;
        a = b;
        b = tmp;
    }
    //Find the gcd
    while(b != 0)
    {
        tmp = a % b;
        a = b;
        b = tmp;
    }
    return a;
}
```

Original algorithm
// Euclidean algorithm
function gcd(a:int, b:int):int
{
    var tmp:int;
    // Swap the numbers so a >= b
    if(a < b)
    {
        tmp = a;
        a = b;
        b = tmp;
    }
    // Find the gcd
    while(b != 0)
    {
        tmp = a % b;
        a = b;
        b = tmp;
    }
    return a;
}

// Euclidean algorithm
function gcd(a:int, b:int):int
{
    var tmp:int;
    // Swap the numbers so a >= b
    if(a < b)
    {
        tmp = a;
        a = b;
        b = tmp;
    }
    // Find the gcd
    while(b != 0)
    {
        tmp = a % b;
        a = b;
        b = tmp;
    }
    return a;
}

Transformed algorithm
/Euclidean algorithm
function gcd(a:int,b:int):int
{
    var tmp:int;
    //Swap the numbers so a >= b
    if(a < b)
    {
        tmp = a;
        a = b;
        b = tmp;
    }
    //Find the gcd
    while(b != 0)
    {
        while (a >= b)
        {
            a = a - b;
        }
        tmp = a;
        a = b;
        b = tmp;
    }
    return a;
}
Deliverables
1- Verilog code
2- Writeup/report in pdf format with synthesis results
3- An FPGA demo: switches and button will be used for inputs and output will be displayed on the seven-segment display.