Objectives
The objectives of this laboratory are:
1. Design various combinational circuits in Verilog and prepare testbeds for them
2. Implement these circuits in Multisim

Multiplexer
Multiplexer is a device that selects one of several input signals and forwards the selected input to the output. Typical multiplexers come in 2:1, 4:1, 8:1 and 16:1 forms. A multiplexer of 2^n inputs has n select lines. When you are generating MUXs, ensure that every possible value for the select signal is accounted for.

![Multiplexer Diagram]

Figure 1: Multiplexer

Deliverables:
1. Create an n bit wide 2:1 mux using the parameter statement.
2. Create a 4 bit wide 2:1 mux by instantiating the n bit wide mux designed above.
3. Simulate the design. Paste the results in the report.

module mux (out, sel, a, b);

//define the parameter
//define the inputs and outputs
//implement the algorithm

endmodule

Demultiplexer
Demultiplexer is in contrast to multiplexer. It takes the information from one line and distributes to number of output lines.
Deliverables
1. Create an n bit wide 1:4 demux using the parameter statement.
2. Create a 4 bit wide 1:4 demux by instantiating the n bit wide demux designed above.
3. Simulate the design. Paste the results in the report.

module demux(in, sel,out);
//define the parameters
//define the inputs and outputs
//implement the algorithm
endmodule

Decoder
A decoder converts N bit binary number to a $2^N$ bit one-hot encoded output such that only one of the output bits is active at one time.

Deliverables
1. Construct a decoder $N \times 2^N$ using the parameter statement
2. Construct a $3 \times 8$ decoder by instantiating the decoder designed above.
3. Simulate the design. Paste the results in the report.

module decoder(in,out);
//parameters defined here
input [n-1:0] in;
output [m-1:0] out;

//algorithm defined here
endmodule

Encoder
Encoder has the opposite functionality of a decoder. Of the n inputs exactly one is assumed to be 1. For example, a 4x2 encoder would have 4 inputs d3,d2,d1,d0 and two outputs e1, e0. For an input 0001, the output is 00, 0010 yields 01 and 1000 yields 11.

**Deliverables**

1. Construct an encoder nxlog2(n) using the parameter statement
2. Construct a 8x3 encoder by instantiating the encoder designed above.
3. Simulate the design. Paste the results in the report.

```verilog
module encoder(in,out);
    //parameters defined here

    input [m-1:0] in;
    output [n-1:0] out;

    //algorithm defined here
endmodule
```