CIS 407/507

Programmable Logic Devices

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Programmable circuits

• Programmable Logic Devices (PLDs)
  ‣ They allow the user to implement the digital logic function of the device
  ‣ They can be reprogrammed for different functions or to resolve bugs
Programmable circuits

- Simple Programmable Logic Devices (PLDs)
  - Read-Only Memory (ROM)
  - Programmable Logic Arrays (PLA)
  - Programmable Array Logic (PAL)

- Structure
  - They have an input connection matrix, which connects the inputs of the device to an array of AND-gates
  - They have an output connection matrix, which connect the outputs of the AND-gates to the inputs of OR-gates which drive the outputs of the device
Read-Only Memory (ROM)

- The input connection matrix is hardwired
- The user can modify the output connection matrix
Programmable Array Logic

- The output connection matrix is hardwired
- The user can modify the input connection matrix
Programmable Logic Arrays

- The user can modify both the input connection matrix and the output connection matrix
**PAL vs. PLA**

- **PLA is the most flexible**
  - One PLA can implement a huge range of logic functions
  - But has large package and higher cost

- **PALs are more restricted**
  - Many device variations needed
  - Cheaper than a PLA
Complex PLDs typically combine PAL combinational logic with Flip-Flops

- Organized into logic blocks
- Fixed OR array size
- Combinational or registered output
- Some pins are inputs only

Usually enough logic for simple counters, state machines, decoders, etc.
Field Programmable Gate Arrays

• FPGAs have much more logic than CPLDs
  ‣ 2K to >10M equivalent gates
  ‣ Requires different architecture
  ‣ FPGAs can be RAM-based or Flash-based
    • RAM FPGAs must be programmed at power-on
      ‣ External memory needed for programming data
      ‣ May be dynamically reconfigured
    • Flash FPGAs store program data in non-volatile memory
      ‣ Reprogramming is more difficult
      ‣ Holds configuration when power is off
FPGA Structure

• Typical organization in 2-D array
  ‣ Configurable logic blocks (CLBs) contain functional logic
    • Combinational functions plus FFs
    • Complexity varies by device
  ‣ CLB interconnect is either local or long line
    • CLBs have connections to local neighbors
    • Horizontal and vertical channels use for long distance
    • Channel intersections have switch matrix
  ‣ IOBs (I/O logic Blocks) connect to pins
    • Usually have some additional C.L./FF in block
FPGA Structure

- Logic blocks
  - To implement combinational and sequential logic
- Interconnect
  - Wires to connect inputs and outputs to logic blocks
- I/O blocks
  - Special logic blocks at periphery of device for external connections
FPGA Structure
FPGA Structure

• Logic block architecture varies between different device families

• Each logic block or cell combines a few binary inputs
  ‣ Typically between 3 and 10
  ‣ With one or two outputs
  ‣ Depending on user specified Boolean logic function

• Cell's combinatorial logic may be physically implemented
  ‣ As a small look-up table memory (LUT)
  ‣ Or as a set of multiplexers and gates
FPGA Structure

• LUT devices tend to be a bit more flexible and provide more inputs per cell than multiplexer cells at the expense of propagation delay

• Logic cells are interconnected by a matrix of wires and programmable switches
Next Class

• System-On-Chip Design